

Programming and physical design tools for flow-based biochips

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A collage of mathematical symbols and formulas. The central element is the Taylor series expansion: $f(x+\Delta x) = \sum_{i=0}^{\infty} \frac{(\Delta x)^i}{i!} f^{(i)}(x)$. Other symbols include a definite integral \int_a^b , a large Greek letter Θ , a square root $\sqrt{17}$, a plus sign $+$, a Greek letter Ω , a delta symbol δ , an exponential function $e^{i\pi}$, an equals sign $=$, a set of curly braces $\{2.7182818284\}$, a Greek letter χ^2 , a summation symbol Σ , a greater-than symbol \gg , a comma $,$, a large exclamation mark $!$, and a pink infinity symbol ∞ .

Programming biochips: vision

- High-level language for describing biological protocols

Original protocol

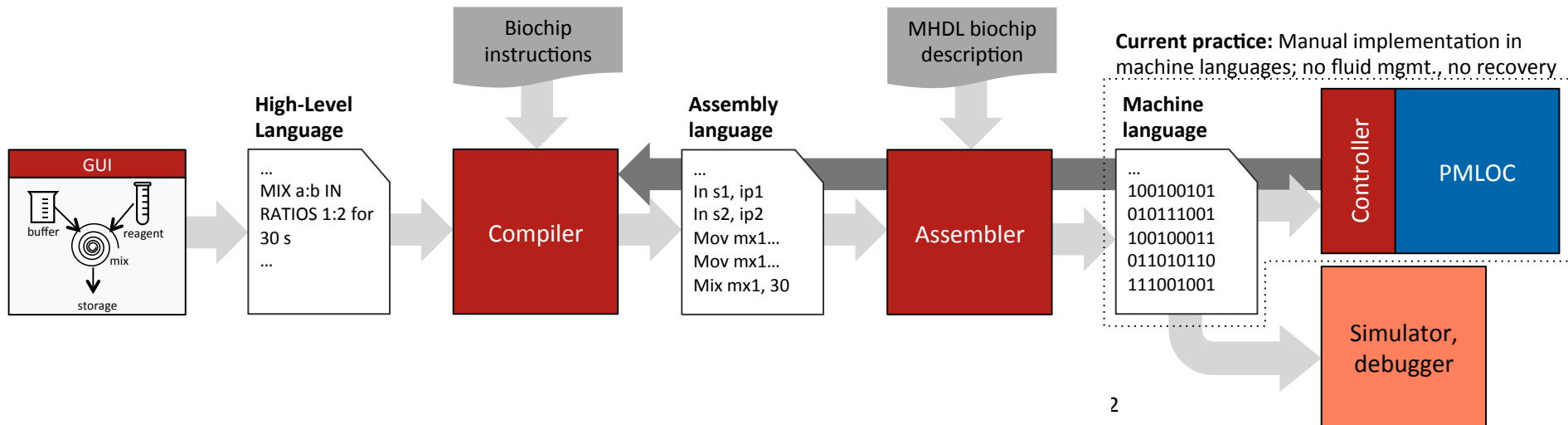
Add 100 ul of 7X Lysis Buffer (Blue) and mix by inverting the tube 4-6 times.

Proceed to step 3 within 2 minutes.

```

1 ASSAY Glucose START
2 fluid Glucose, Reagent, Sample;
3 fluid a, b, c, d, e;
4 VARResult[5];
5 input Glucose 50;
6 input Reagent;
7 input Sample 30;
8 conflict Sample FOLLOWS Glucose WASH
  water;
9 a=MIX Glucose AND Reagent IN RATIOS1 : 1
    
```

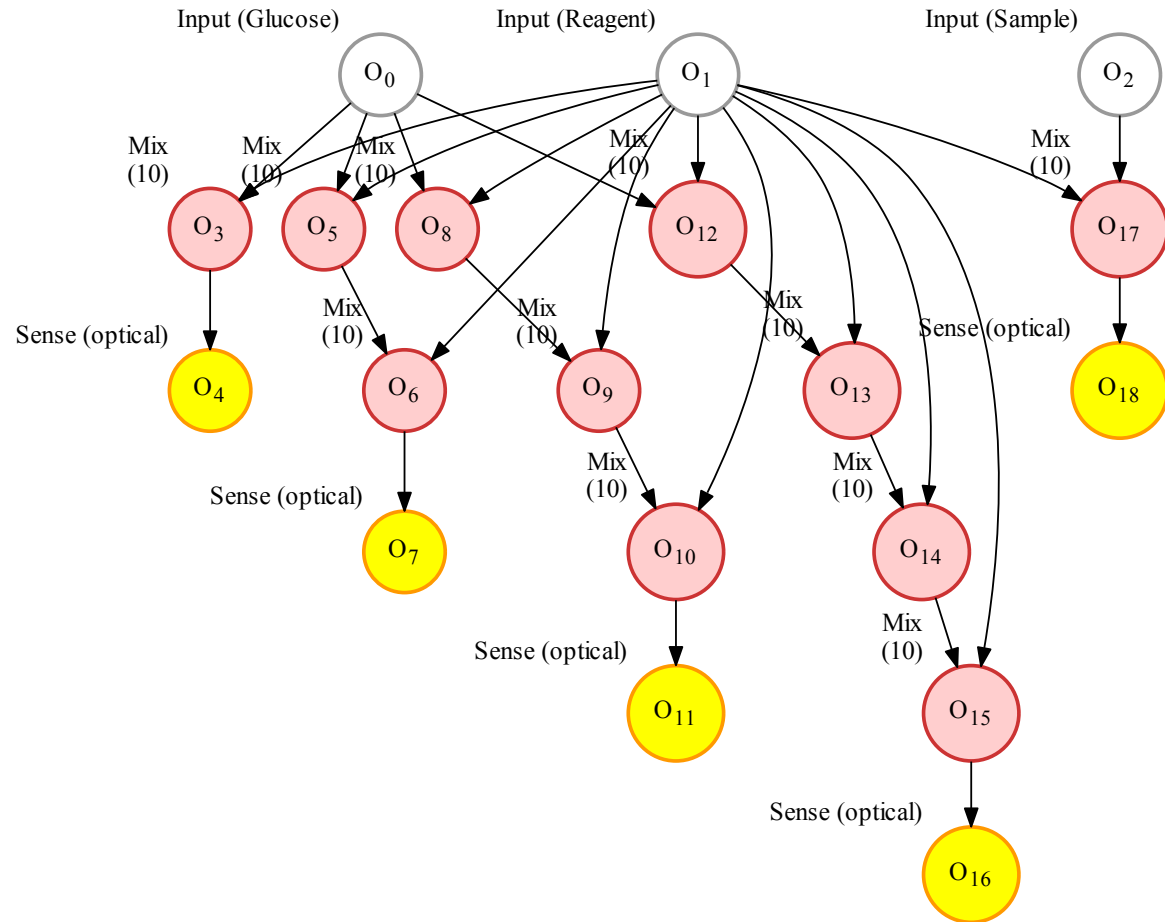
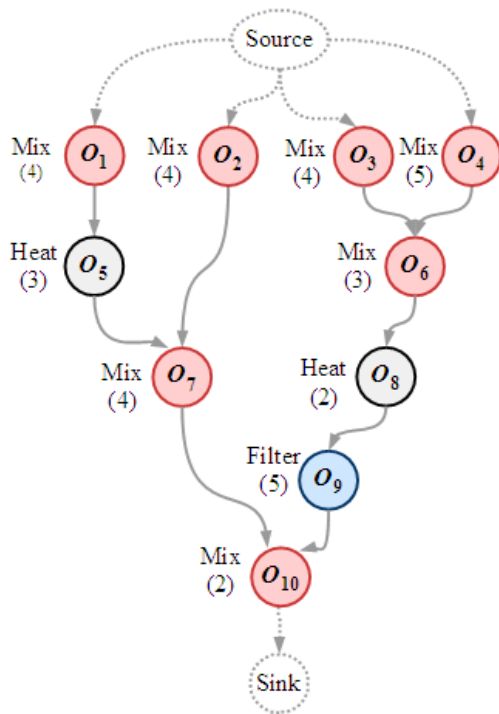
- Programming tools: compiler, assembler, debugger, simulator



2

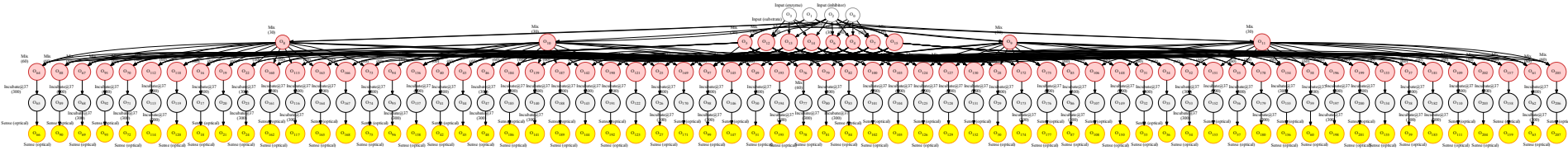
From HLLs to graph models

- We model a biochemical application as a graph
- Compiler: translates the protocol written in the HLL into the graph, doing mixing optimization

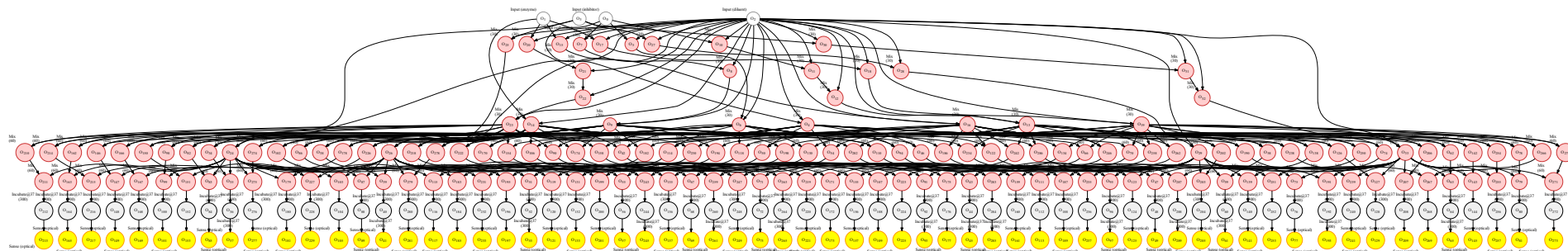


The graph model for an enzyme test

- Considering a **variable** mixer module

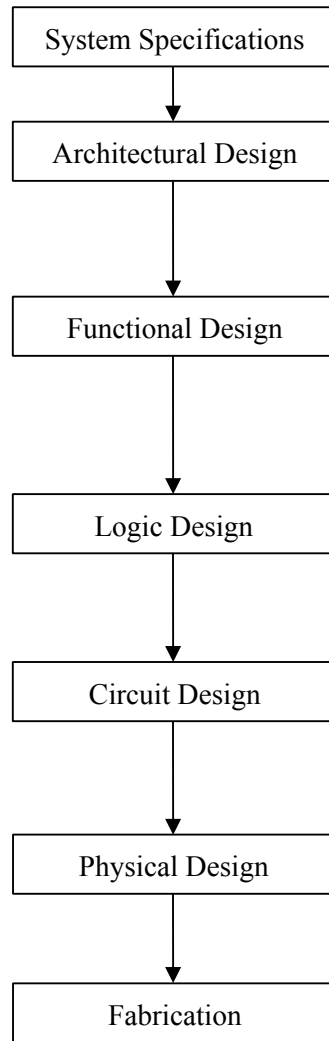



- Considering a **1:1** mixer module; mixing is optimized



Physical design: VLSI vs mVLSI


VLSI




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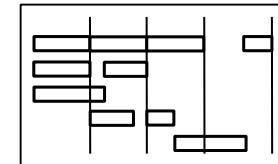
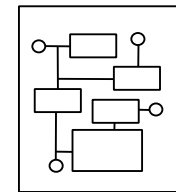
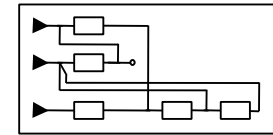
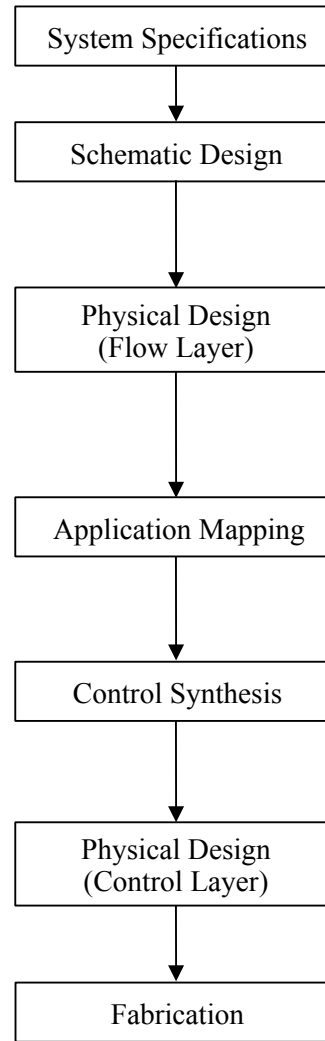
$$X = (AB + CD)$$

$$Y = (A(B+C))$$

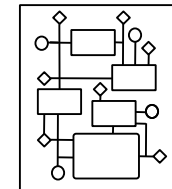
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mVLSI

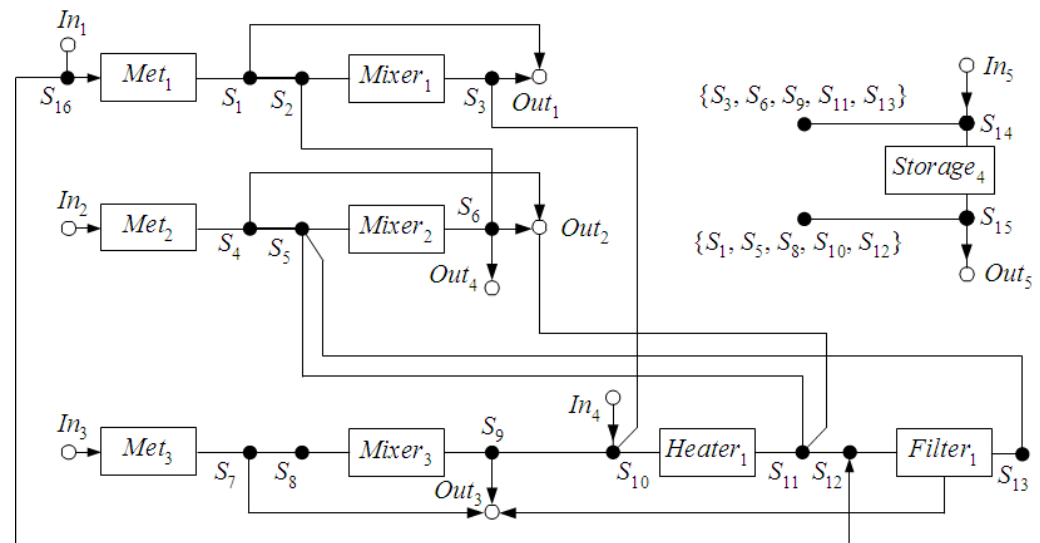
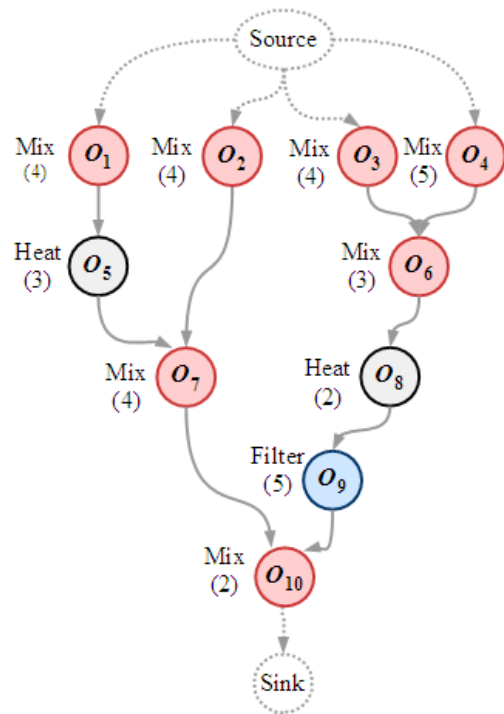


	t1	t2	t3	...
v1	0	1	0	...
v2	1	0	0	...
...



Allocation and schematic design

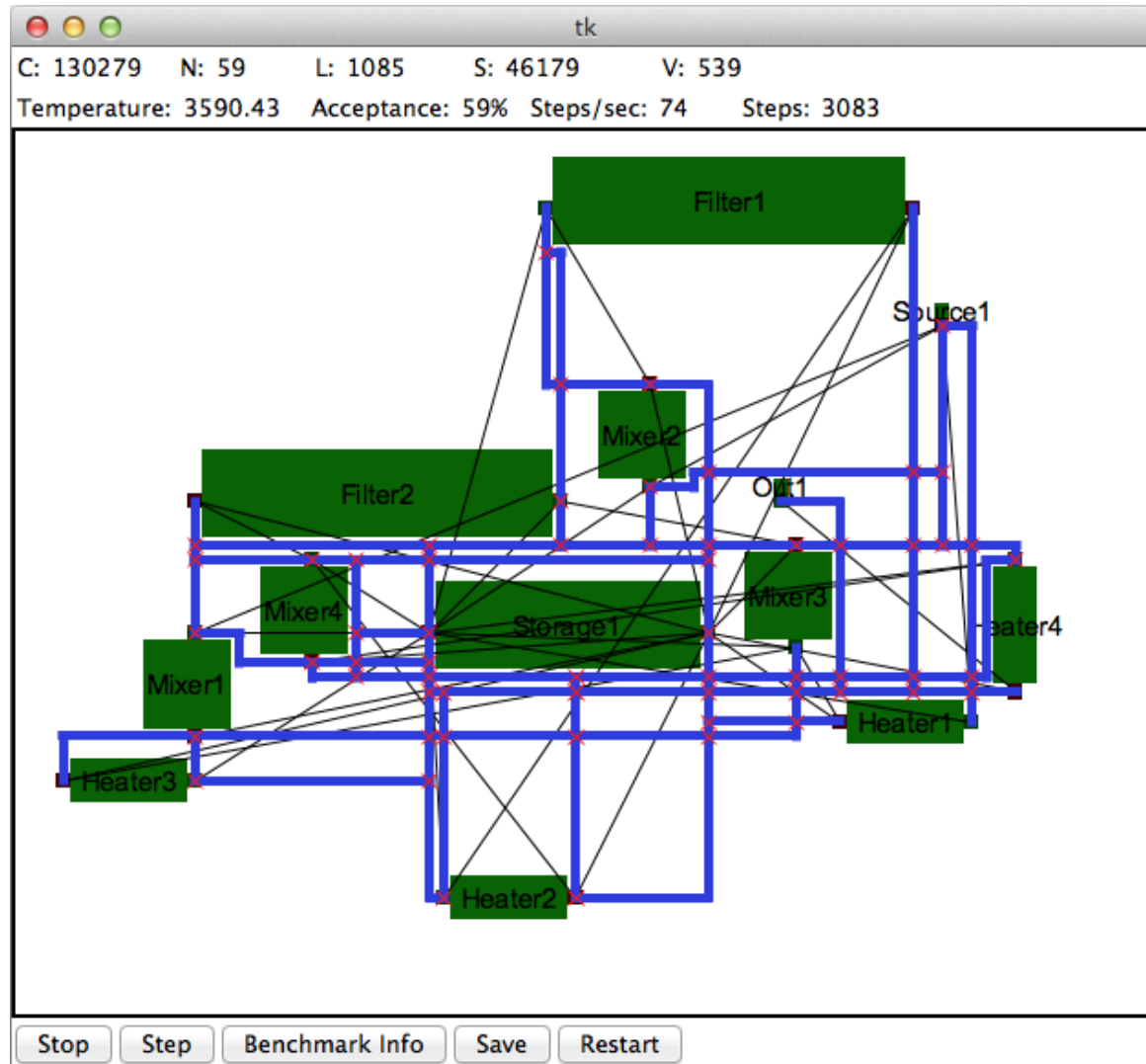
- How many components, and how to interconnect them?



Mixer	3
Heater	2
Filter	1

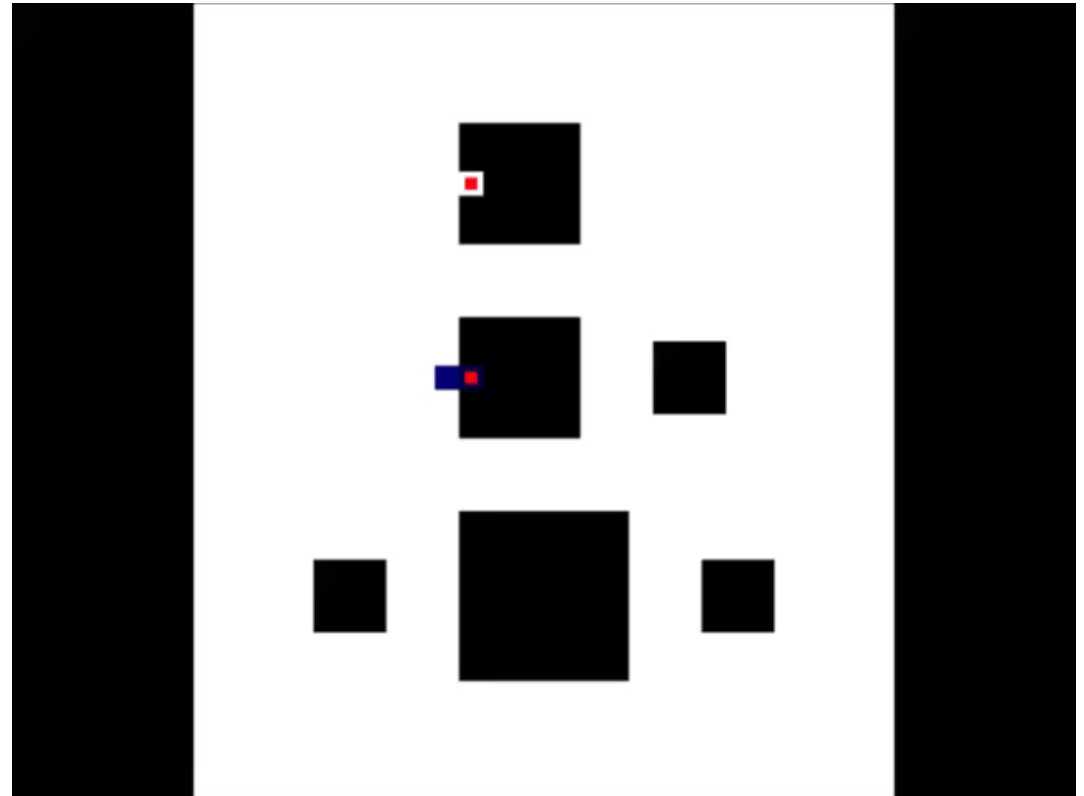
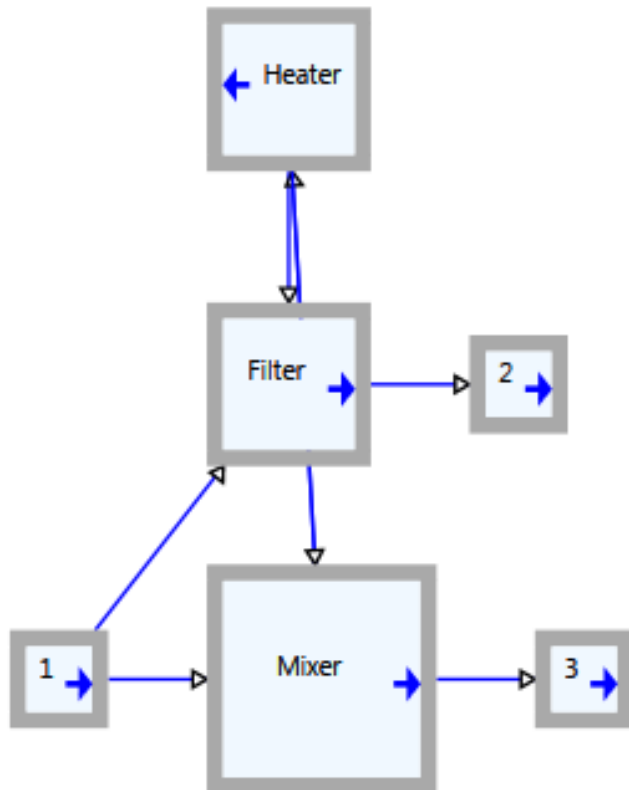
- Input/ output ports
- Storage units
- Fluidic constraints

Flow layer placement



Flow-channel routing

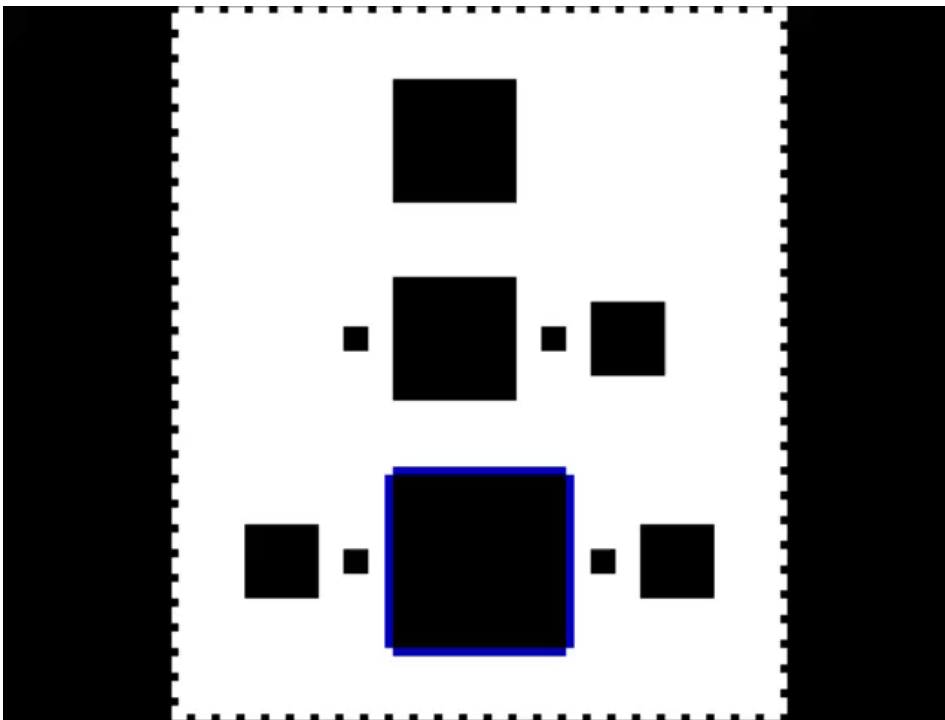
- Algorithms
 - Lee, Hadlock, Soukoup



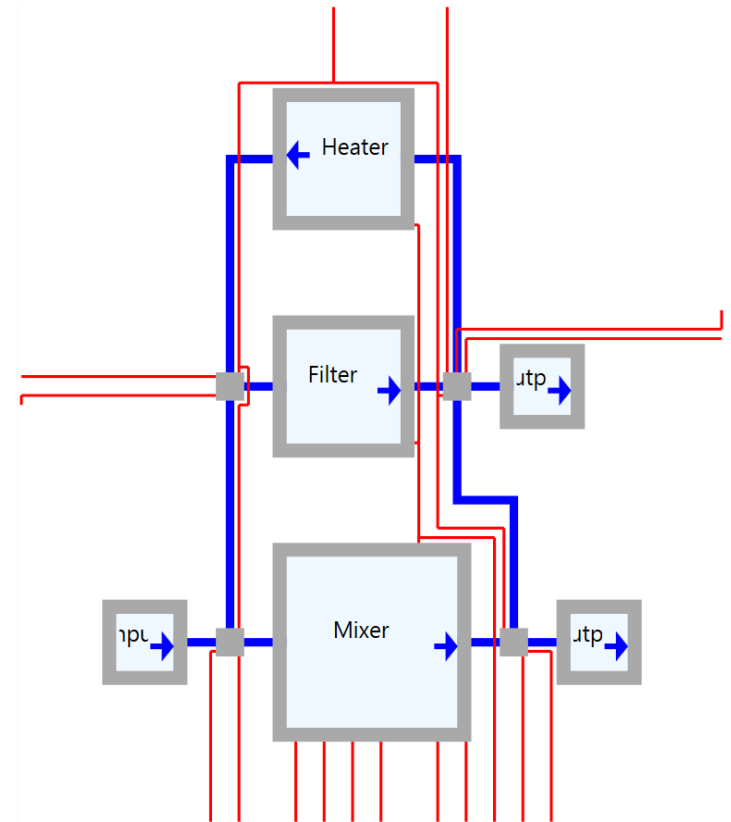
Control layer routing

- Algorithms

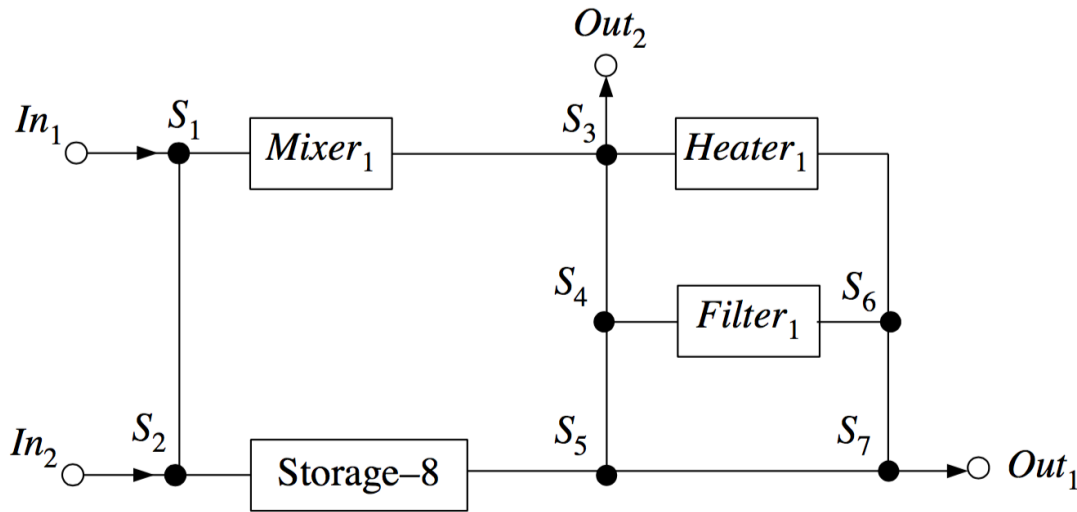
- Lee-Steiner: Route from component to nearest air inlet; rip-up and reroute
- PathFinder



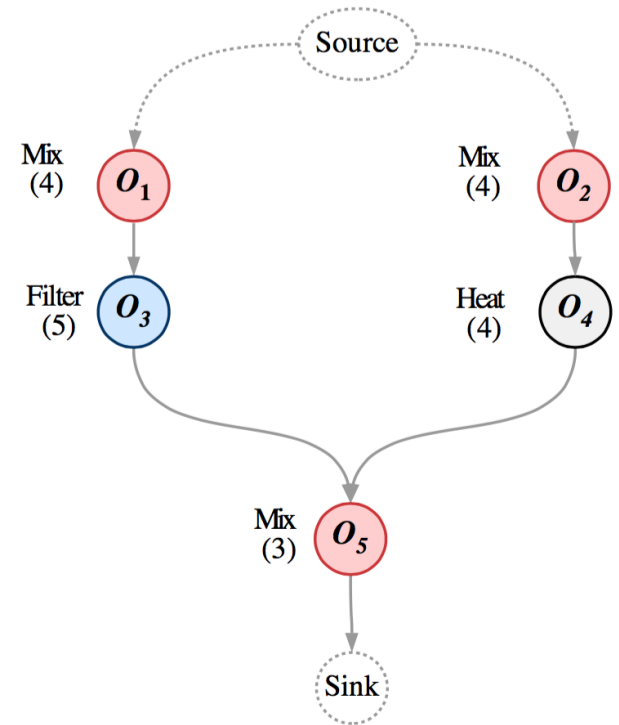
Lee-Steiner's algorithm



Design for fault-tolerance: motivation example

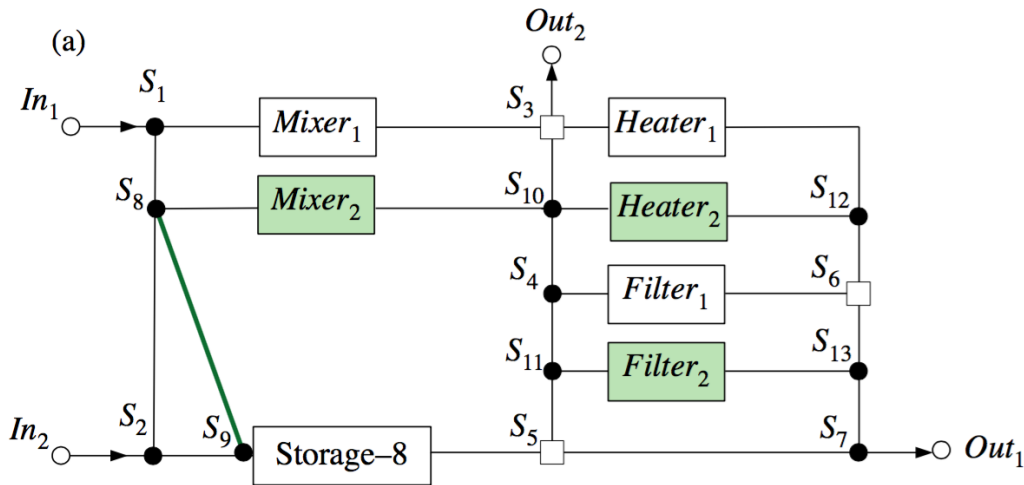


Architecture without fault-tolerance

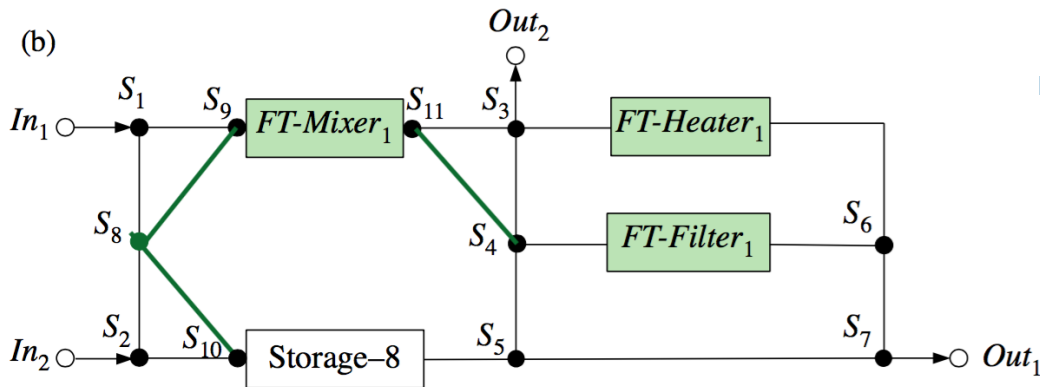


Application

Straightforward vs. optimized redundancy



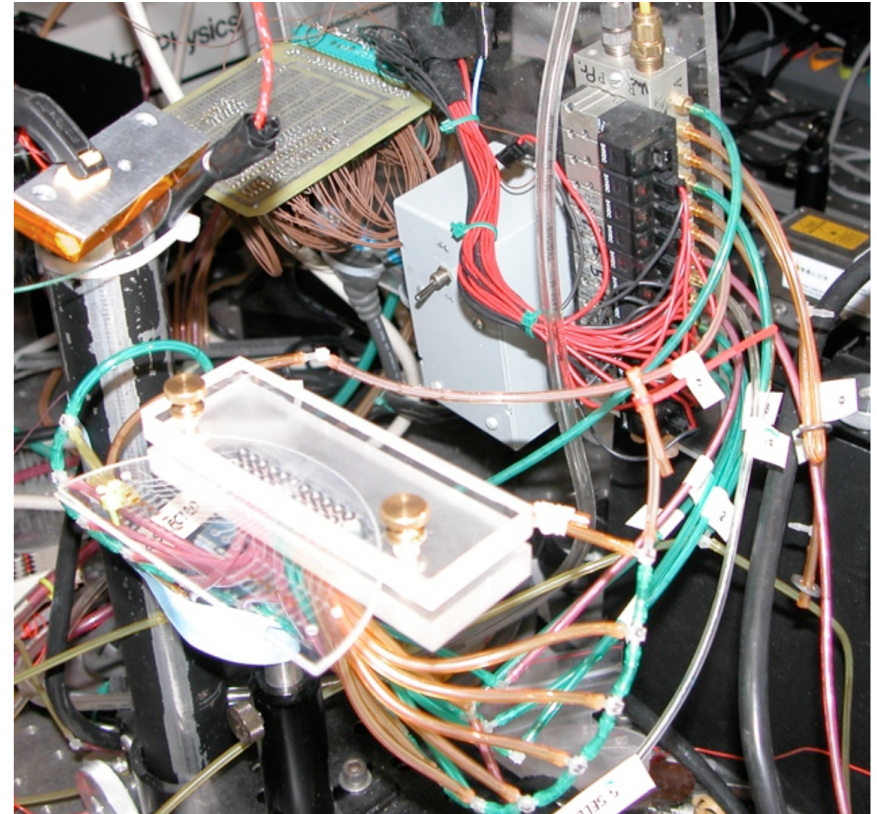
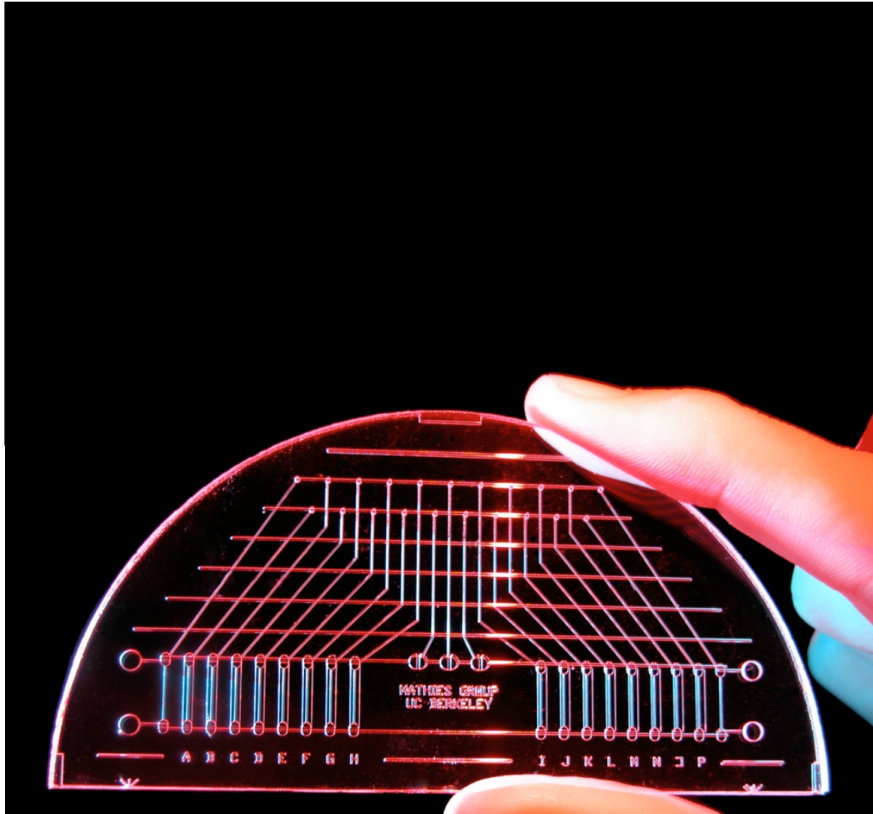
- Straightforward solution: redundancy not optimized; architecture cost: 129



- Optimized solution the introduction of redundancy is optimized; architecture cost: 96

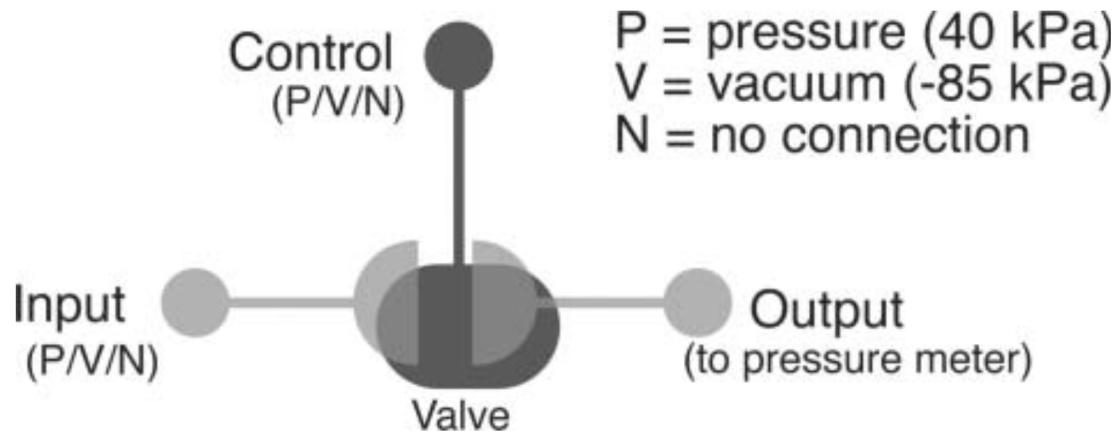
The need for on-chip control

- Slide from Prof. William Grover

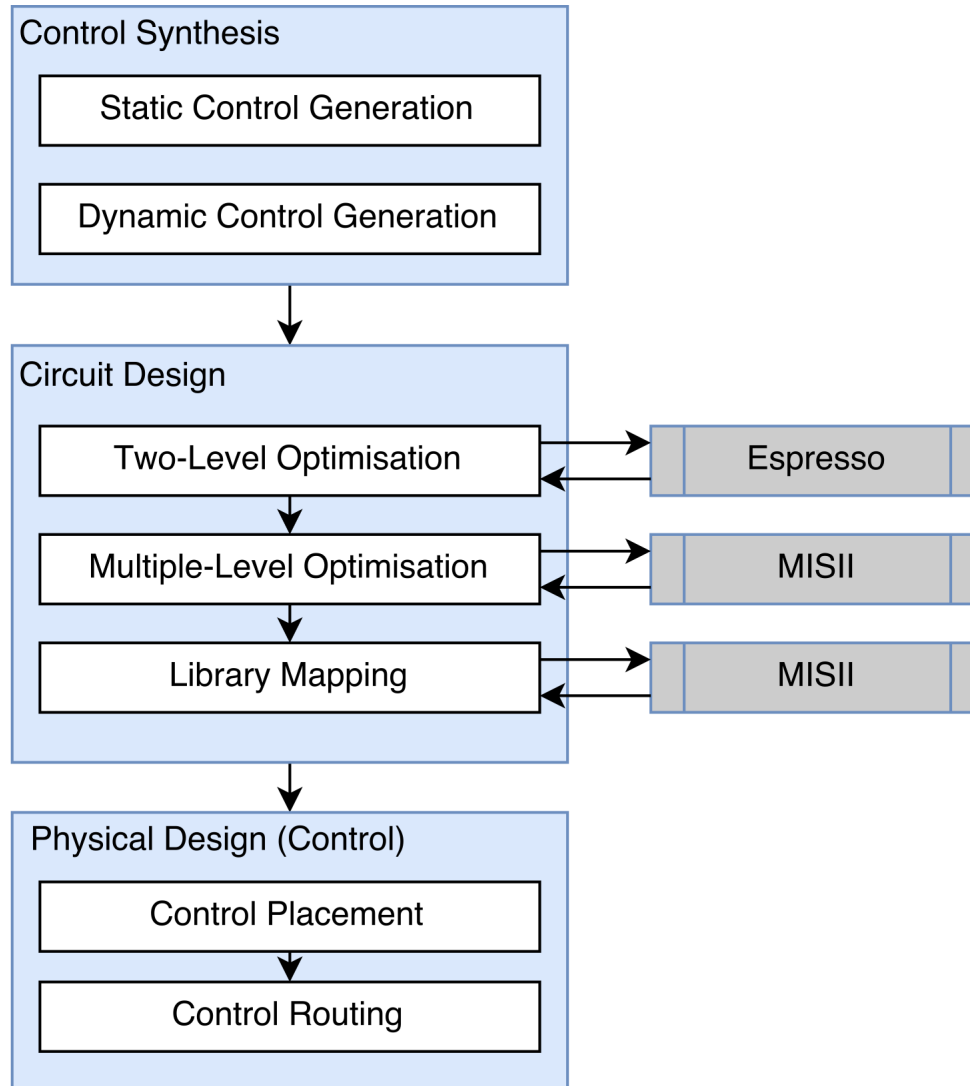


On-chip control

Rule	Maintained at input/kPa	Maintained at control/kPa	Measured at output/kPa
PP	40	40	0
PV	40	-85	40
PN	40	0	40
VP	-85	40	0
VV	-85	-85	-83
VN	-85	0	0



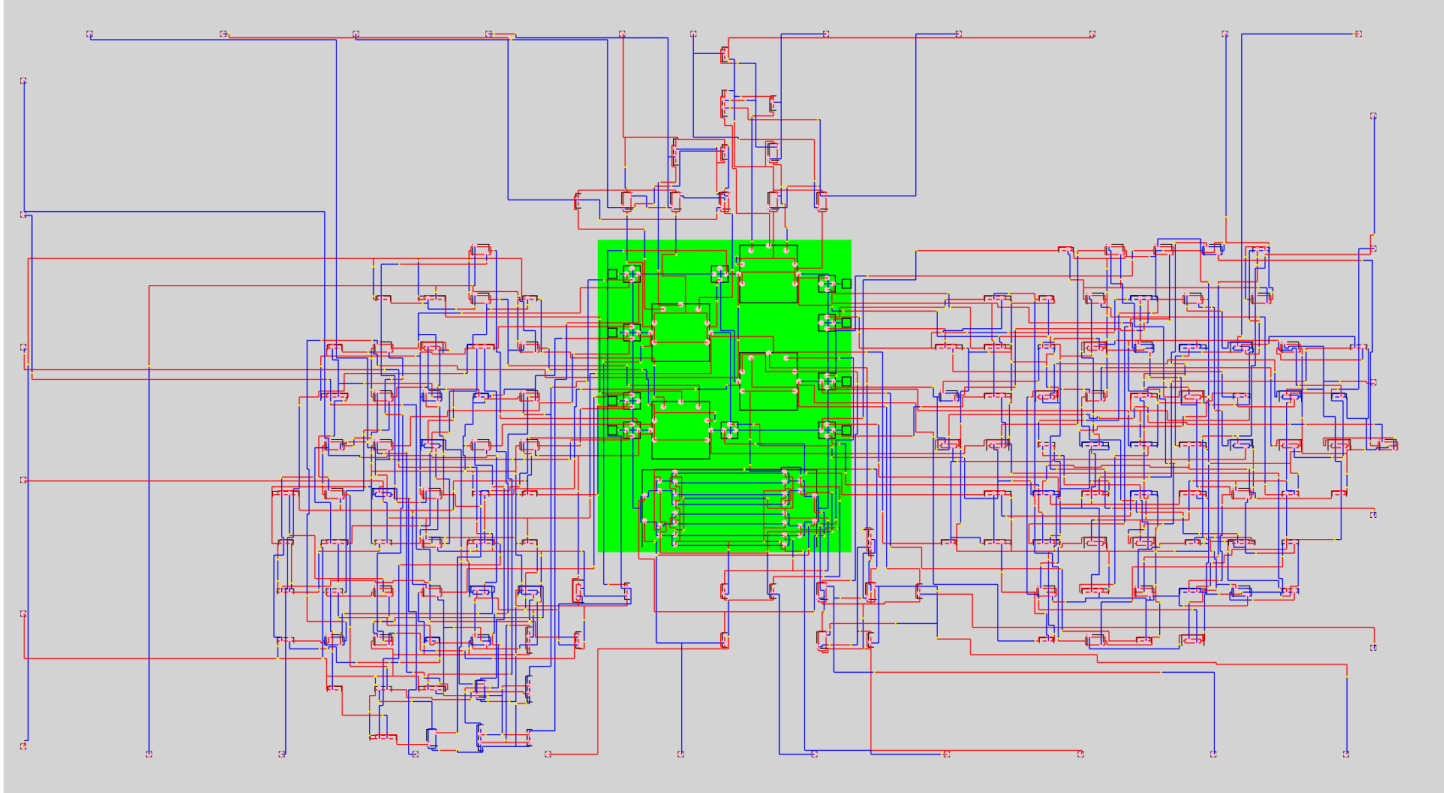
Control circuit synthesis...



..and its physical design

MainWindow

Flow Placement	Size of Flow	20800
Flow Routing	Size of Control	301512
Control Placement	Ratio	14.4957692307692
Control Routing	# Pressure Sources	32
Breadth First Search	# Flow components	23
Reduce Chip Size	# Valves	96
Save	# Control Components	142
Load	Length of Flow	447
Random Seed	Length of Control	35319
Seed	Number of Layer Changes	752
200		
Alpha		
0.9999		
Iterations		
10000		
Starting Temperature		
10		
Final Temperature		
3.678610		
0		



0